Preprint: 2001 IEEE International Integrated Reliability Workshop (IRW)

On the Nature of Ultra-thin Gate Oxide Degradation During Pulse Stressing of nMOSCAPs

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Abstract

Preliminary Pulse (dynamic) stress testing (PVS) results performed in accumulation indicate that degradation and breakdown mechanisms occur such as stress induced leakage current (SILC) and hard breakdown (HBD) as previously reported [1-3]. Additional degradation and breakdown mechanisms due to PVS were observed for the first time such as soft breakdown (SBD), limited hard breakdown (LHBD) and moderate breakdown (MBD). Finally, post-PVS induced LHBD I-V measurements show the leakage current in accumulation is more than 5 orders of magnitude greater than in inversion at similar voltages.

Introduction

For SRAM applications, the bias condition of a transistor in the off-state is in accumulation. Furthermore, voltages applied to transistors in SRAM are not constant but are digital. For reliability concerns, it is important to determine the worst-case bias condition relative to inversion and accumulation, and to do so using pulsed voltage stressing (PVS), which better emulates digital operation. We (unpublished) and others [4] have observed that breakdown in accumulation occurs at lower breakdown voltages than in inversion. Hence, reliability of SRAM devices using ultrathin gate dielectrics may be more of a concern when operated in accumulation than in inversion. In this paper, we examine the nature of degradation and breakdown mechanisms of nMOSCAPs under PVS in accumulation.

Experimental Procedures

Degradation and breakdown mechanisms in ultrathin SiO_2 were studied and compared between unipolar PVS and constant voltage stressing (CVS) in accumulation. Current-voltage measurements before and after stressing were performed to determine the extent of oxide degradation and the character of oxide breakdown mechanisms. During PVS, the stress voltage and pulse period were –5.5V and 1s, respectively. The pulse widths used during PVS were 100ms (10% duty cycle) and 50ms (5% duty cycle). The stress voltage on the gate during CVS was –5V and -5.5V. Pre- (i.e., on fresh capacitors) and post-stress I-V measurements were performed from 0 to –2V so as not to induce further stress. Post-PVS I-V measurements were performed following a range of pulses from 1 to 50 pulses. Post-HBD I-V measurements were carried out to compare I-V characteristics in inversion and accumulation (0 to ±8V) and to examine MBD. PVS was continued beyond the initial HBD to observe any further degradation behavior.

The test and measurement apparatus used included a HP 4155A semiconductor parameter analyzer (SPA) and an Agilent 4156C High Precision SPA equipped with Cascade Microtech DC micropositioners with 50 Ω triaxial connections. Samples and micropositioners were placed in a Faraday cage. All measurements were performed on nMOSCAPs in which the gate oxide thickness, t_{ox}, and area, A_{ox}, were 3.2nm and $2.1 \times 10^{-4} cm^2$, respectively.

Results

Figure 1 shows the I-V characteristics in accumulation (0 to -2V) of an unstressed capacitor and a capacitor stressed after multiple sets of pulse stresses. The initial post-PVS I-V measurements demonstrate oxide degradation in the form of SILC. Other data (not shown here) show SILC increasing with each additional pulse stress. Further PVS produces I-V data that is characteristic of SBD, which has been reported for CVS or CCS but for PVS induced SBD to the authors' knowledge. Moreover, a seemingly softer SBD initiated by PVS was observed (figure 1-2). Additional PVS caused HBD. Further sets of pulses after the first HBD event did not reveal SILC-like behavior. I-V measurements in inversion showed the leakage current was at least 5 orders of magnitude lower than a similar voltage range in accumulation (figure 2). Increasing the voltage range in accumulation (0 to –8V) exposed noisy breakdown events (termed MBD) beginning at –3V and reaching current compliance at just over –6V (figure 2). A subsequent I-V measurement (0 to –8V) indicated that the SiO_2 had completely broken down (figure 2).

SBD was observed in pulse ranges of 25 to 225 while HBD was observed in pulse ranges of 200 to 425 (figure 3). Post-SBD leakage currents at –2V, induced by PVS, were at least 2 orders of magnitude greater than leakage currents at –2V in fresh capacitors. Similarly, post-HBD leakage currents at –2V were 2 to 3 orders of magnitude greater than SBD leakage currents. SBD was observed more often during 5% duty cycles than during 10% duty cycles.

CVS and pre- and post-CVS I-V data are shown in figure 4. A SBD event is readily observed. The CVS test was interrupted at several intervals and I-V measurements taken. The resulting data are indicative of SILC and SBD. The I-V data taken in the CVS induced SBD region appear to be more dispersed (figure 4) than for the IV data taken in the PVS induced SBD region (figure 1).

Discussion and Summary

A phenomenon that this group has observed in I-V data following HBD during CVS and PVS is a further breakdown of the oxide at higher voltages. The I-V measurement procedure used following stress testing (CVS or PVS) is to use a low voltage range to limit further degradation. However, when the voltage range is increased to include voltages up to –8V, a noisy breakdown phenomenon is observed until the maximum current compliance of the SPA is reached (0.1A) and complete HBD results. HBD is apparent when a subsequent I-V measurement is performed and a smooth but greater leakage current is observed. We term the noisy breakdown moderate breakdown (MBD), since it occurs before complete HBD. Thus, the HBD observed in the 0 to –2V range is a limited HBD or LHBD. Both LHBD, MBD and HBD are shown in figures 1 and 2. HBD is observed for both CVS (figure 4) and PVS (figures 1-2). To the authors' knowledge, MBD has not been reported with regard to PVS, yet a somewhat similar I-V response following CVS or voltage ramped stress can be seen in the data of Nafría *et al.* and Lombardo *et al.*[5, 6]. MBD is primarily the result of LHBD caused by limiting the current compliance of the measurement

system. By limiting the compliance, the power to the capacitor is restricted and the breakdown of the oxide is incomplete. MBD may be a reliability issue if the circuit acts as compliance limit [7].

Although asymmetry in the I-V data following LHBD (-8 to +8V) has been observed following CVS [8], to the authors' knowledge, asymmetry due to PVS (figure 2) has not been reported. It is interesting to note that the leakage in inversion following HBD is on the order of leakage attributed to SBD in accumulation. The large difference in leakage current between inversion and accumulation following HBD may be do to factors such as: 1) electron injection from the gate is greater than from the substrate because the poly-Si/SiO_2 interface is more defective than the substrate-Si/SiO_2 interface; 2) minority carrier concentration in inversion at an equivalent oxide voltage is less than an equivalent majority carrier concentration in accumulation; 3) voltage across the oxide at equivalent gate voltages is asymmetric with respect to accumulation and inversion.

Preliminary PVS results indicate that degradation and breakdown mechanisms occur such as SILC and HBD. Furthermore, additional degradation and breakdown mechanisms due to PVS were observed for the first time such as SBD, LHBD and MBD. This indicates that the breakdown mechanisms observed may occur during the off-state in devices and may be a reliability concern.

Future work will entail additional frequency dependent PVS, pulse to breakdown conversion to equivalent time to breakdown, and additional studies of LHBD and its induced IV asymmetry and MBD.

W.B.K. would like to acknowledge the Idaho Governor's High Tech Initiative, SRC Education Alliance and Tom Paquette of Insight Analytical Labs for stimulating his interest in this subject.

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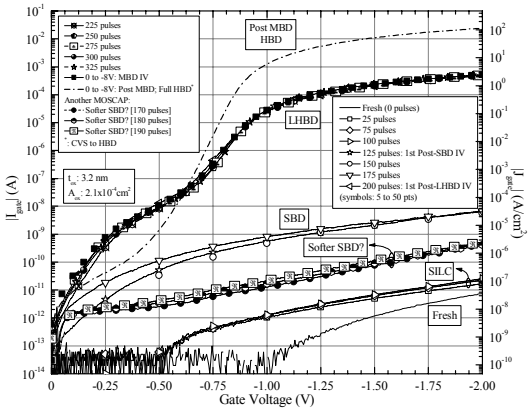

Figure 1: Pre- and post-PVS *I-V* data showing SILC, possible softer SBD, SBD, LHBD and complete HBD.

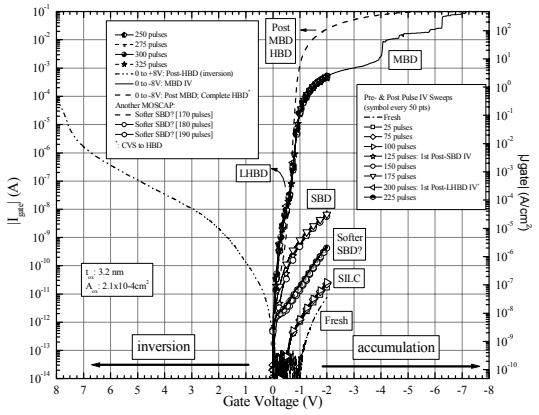

Figure 2: Similar to figure 1, but in addition, showing MBD and asymmetry of the I-V data with regards to inversion versus accumulation following HBD.

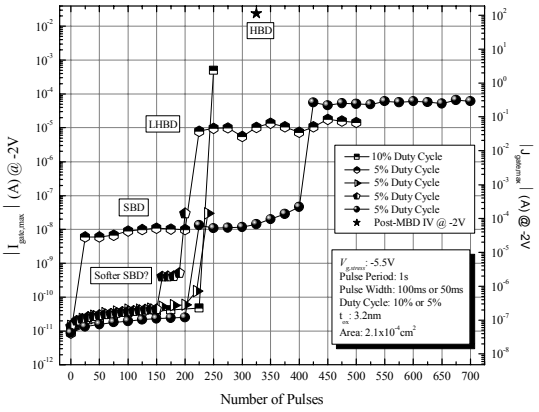

Figure 3: Current at –2V versus number of pulses at 5 and 10% duty cycles. Evident is SILC, soft SBD, SBD and LHBD. HBD after MBD is shown for comparison.

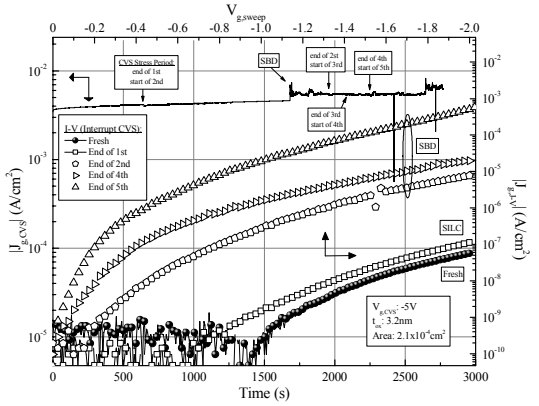

Figure 4: CVS *J-t* plot showing SBD and the intervals in which *J-V* measurements were performed. Corresponding *J-V* plots demonstrating SILC and SBD (symbol every 5 points).